

SANYO

No.1374E

CMOS IC

LC7533**3V Electronic Volume Control****Use**

- Attenuation of signal

Features

- CMOS process 3V typ. operation
- Up/down operation is performed with SW input.
- 4-bit, 16-step counter. Step 6* is set with initial input ($\overline{\text{INIT}}$).
- Center tap provided.
- Maximum attenuation : - 60dB or less
- Attenuation curve : Pseudo curve A. Left/right simultaneous setting.
- * : Step 6 means mode 6.

Absolute Maximum Ratings at Ta = 25°C

| | | | unit |
|-----------------------------|--------------|----------------------|------|
| Maximum Supply Voltage | V_{DD} max | V_{SS} to 6 | V |
| Supply Voltage | V_I | V_{SS} to V_{DD} | V |
| Allowable Power Dissipation | P_d max | 100 | mW |
| Operating Temperature | T_{opr} | - 30 to + 75 | °C |
| Storage Temperature | T_{stg} | - 40 to + 125 | °C |

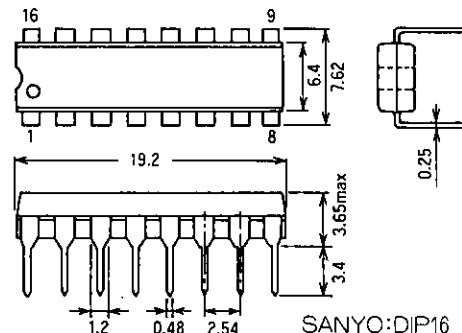
Allowable Operating Conditions at Ta = 25°C

| | | | unit |
|-------------------------|-----------|---|-------------------------|
| Supply Voltage | V_{DD} | 2.1 to 5.0 | V |
| Input 'H'-Level Voltage | V_{IH1} | $\overline{\text{INIT}}, \text{CE pin}$ | $0.7V_{DD}$ to V_{DD} |
| | V_{IH2} | $\overline{\text{UP}}, \overline{\text{DN}}, \text{CR pin}$ | $0.9V_{DD}$ to V_{DD} |
| Input 'L'-Level Voltage | V_{IL1} | $\overline{\text{INIT}}, \text{CE}$ | 0 to $0.3V_{DD}$ |
| | V_{IL2} | $\overline{\text{UP}}, \overline{\text{DN}}, \text{CR}$ | V_{SS} to $0.1V_{DD}$ |

Electrical Characteristics at Ta = 25°C

| | | | min | typ | max | unit |
|----------------------------|----------------|--|-----|-----|------|------|
| Signal Distortion | THD_1 | $V_{DD} = 3V, R_L = 50k\Omega, f = 1kHz$ | | | 0.5 | % |
| | THD_2 | $V_{DD} = 2.1V, R_L = 50k\Omega, f = 1kHz$ | | 1 | | % |
| Output at Attenuation Mode | X_{OUT} | 0dBm input, 1kHz, 51k Ω load | | | - 60 | dB |

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Package Dimensions 3006B-D16IC
(unit: mm)

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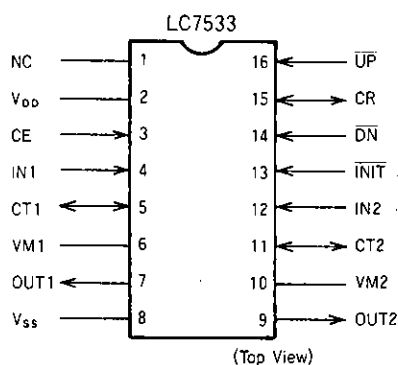
LC7533

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| | | | min | typ | max | unit |
|----------------------------|---|--|-----|-----------|-----|---------------------|
| Signal Transmit Delay Time | t_d | Between IN and OUT, no load | | 1 | | μs |
| Input Impedance | r_i | $\overline{\text{UP}}, \overline{\text{DN}}, \text{CE}$ only | 100 | | 400 | $\text{k}\Omega$ |
| Output Noise Voltage | V_{NO} | $V_{\text{DD}} = 3\text{V}, R_L = 50\text{k}\Omega, \text{STEP "0"}$ | | | 8 | μV |
| Input 'H'-Level Current | I_{IH} | CE pin, $V_{\text{DD}} = 3\text{V}, V_I = 3\text{V}$ | | | 40 | μA |
| Input 'L'-Level Current | I_{IL} | $\overline{\text{UP}}, \overline{\text{DN}}$ pin, $V_{\text{DD}} = 3\text{V}, V_I = 0\text{V}$ | -55 | | | μA |
| Attenuation Balance | ΔV | Pins OUT1,2, other than STEP "0" (Note 1) | -2 | 0 | 2 | dB |
| Channel Balance | ΔV_0 | Between pins OUT1,2, other than STEP "0" (Note 2) | -2 | | 2 | dB |
| Current Dissipation | I_{DD} | $V_{\text{DD}} = 3\text{V}, \text{CE} = V_{\text{DD}}, \overline{\text{INIT}} = V_{\text{DD}},$ other pins : OPEN | | | 1 | mA |
| | \overline{I}_{DD} | $V_{\text{DD}} = 3\text{V}, \text{CE} = V_{\text{SS}}, \overline{\text{INIT}} = V_{\text{DD}},$ other pins : OPEN | | | 1 | μA |
| Crosstalk between Channels | CT | $V_{\text{DD}} = 1.5\text{V}, V_{\text{SS}} = -1.5\text{V}, V_M = 0\text{V},$ $f = 1\text{k}\Omega, 1\text{V}_{\text{rms}}$ input, test side input : $1\text{k}\Omega$ short | | 85 | | dB |
| Minimum Pulse Width | $T_{\text{UP/DN}}$ T_{INIT} | $T = (\text{CR oscillation cycle}) \overline{\text{UP}}, \overline{\text{DN}}$ pin INIT pin | | 1.5T 2 | | ms μs |

Note 1 (1) $\Delta\text{V} = 20\log_{10} V_{\text{OUT}}/V_{\text{TYP}}$
 V_{OUT} : OUT1 (OUT2) output level
 V_{TYP} : Standard output level
 (2) Satisfy $V_{\text{OUT}}(\text{STEP } N) < V_{\text{OUT}}(\text{STEP } N + 1)$
 Note 2 (1) $\Delta\text{V}_0 = 20\log_{10} V_{\text{OUT1}}/V_{\text{OUT2}}$

Pin Assignment



Note 1 : No bonding exists on the inside of NC pin. It is recommended that the outside should be shorted to $V_{\text{DD}}, V_{\text{SS}}$, etc. on the printed circuit board.

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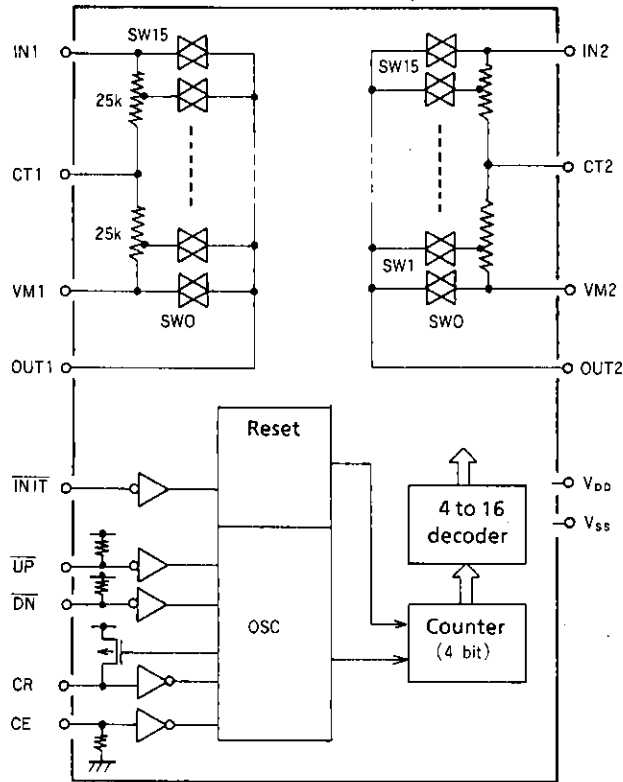
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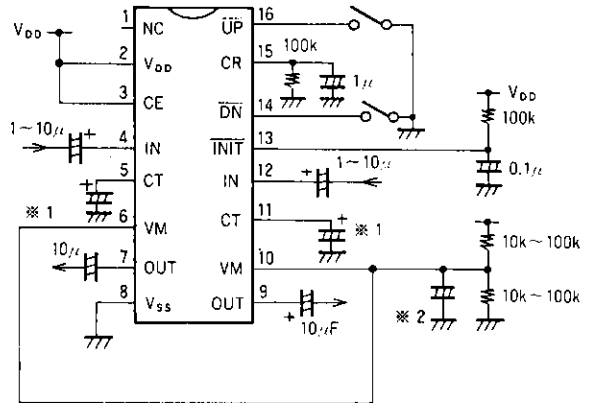
Equivalent Circuit Block Diagram

[Common to LC7533]



Note 1 : The TEST pin is bonded only when the MFP20 is used.

Sample Application Circuit [LC7533 DIP16]



For V_M , $1/2V_{DD}$ bias is recommended.

- ※1 For low-band boost (approx. $1\mu\text{F}$)
- ※2 The larger the capacity is (approx. $100\mu\text{F}$), the better the characteristics of attenuation and crosstalk.

Unit (resistance: Ω , capacitance: F)

Pin Description

| Pin Name | Pin Number | Description |
|--------------------------|------------|---|
| IN1, IN2 | 4, 12 | Input pin for volume control |
| OUT1, OUT2 | 7, 9 | Output pin for volume control |
| V_{M1}, V_{M2} | 6, 10 | Bias pin. When operated form single supply, $1/2V_{DD}$ is applied to this pin. |
| CT_1, CT_2 | 5, 11 | Tap pin provided at the center of volume control. By connecting C and R to this pin, the loudness can be controlled. |
| CE | 3 | When this pin is set to "L", the current dissipation is reduced. This pin must be "L" at backup mode. |
| $\overline{\text{INIT}}$ | 13 | Initial pin. When set to "L", the 6th step is reached. |
| $\overline{\text{UP}}$ | 16 | When the level on this pin is made to fall, the step rises and the volume goes up. When held at "L", the volume goes up; if set to "H", the volume stops going up at a step reached at that moment. The step stops at the MSB position. |
| $\overline{\text{DN}}$ | 14 | The $\overline{\text{DN}}$ operation is the reverse of UP. When the $\overline{\text{UP}}, \overline{\text{DN}}$ are set to "L" at the same time, the $\overline{\text{UP}}$ is given priority. The step stops at the LSB position. |
| CR | 15 | Pin for connecting R, C on which the rate of step depends. |
| V_{DD} | 2 | Power supply pin (+) |
| V_{SS} | 8 | Ground |
| NC | 1 | No bonding exists on the inside of NC pin. Connected to V_{DD} or V_{SS} is recommended. |